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Polymer and Organic Nonvolatile Memory Devices†

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Organic molecules and semiconductors have been proposed as active part of a large variety of nonvolatile memory devices, including resistors, diodes and transistors. In this review, we focus on electrically reprogrammable nonvolatile memories. We classify several possible devices according to their operation principle and critically review the role of the π-conjugated materials in the device operation. We propose specifications for applications for organic nonvolatile memory and review the state of the art with respect to these target specifications. Conclusions are drawn regarding further work on materials and device architectures.

1. Introduction

The main drive to develop organic nonvolatile memory is currently for applications of thin-film, flexible or even printed electronics. By thin-film technologies, electronic functionality can be foreseen in very large quantity and at very low cost on substrates such as plastic and paper. Items where today integration of a silicon chip is not economical, such as toys, cards, labels, badges, value paper, and medical disposables, could be imagined to be equipped with electronics—and memory.

The simplest nonvolatile memory for such applications could be a so-called hard-wired memory, where the bits are defined as permanently present conductive lines at the time of production of the memory. Technologies to make such memory can be printing of conductive lines (additive), or ablation of unwanted lines (subtractive). A second memory type are write-once read-many memories, known as WORM, where the bits can programmed at the site of use, albeit only once. WORM can be implemented by fuses (in which all lines are made conductive during production and selectively fused at the site of use), or antifuses (lines made conductive at the site of use). Reproducible and reliable fuse technology by π-conjugated material has been shown using camphorsulfonic-acid-doped polyaniline[1] and poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS).[2,3]

The most versatile type of memories are reprogrammable and demand a mechanism of repeatable switching between different states. Light has been used for erasing memory devices, e.g., in the erasable programmable read-only memory, EPROM. However, the most convenient mechanism will be reprogrammability by voltage or current, i.e., the electrically erasable and programmable nonvolatile memory. In this paper, we limit the discussion to this type of memory.

In a stand-alone memory, the array of memory bits has contact pads at its periphery, and an external piece of hardware is required to program the array, as well as to read it out. For some applications this may be sufficient, but clearly it is desirable that a memory array can be integrated on chip with read-out electronics and preferably also with electronics to write the array—the writing operation usually requiring larger voltages and currents than the read operation. This calls for memory technologies that can be embedded in the logic.

Detailed specifications of thin-film nonvolatile memory arrays will depend on the application, but it may be expected that the requirements for this type of memory will be in the ranges suggested in Table 1.

In the paper, we provide an overview of the device concepts that have been proposed in past years to realize such electrically reprogrammable thin-film nonvolatile memory arrays, specifically using conjugated semiconductors and mostly compatible with organic thin-film transistors. These principles are not new to the field of organic electronics; they have been pioneered in silicon technology, and are being or have been used there.

NAND flash is the dominant nonvolatile memory technology in silicon, reputed for long retention and high density at low cost. The operation of a flash transistor is based on charge storage on a floating gate or in a gate dielectric of a transistor structure. A similar structure can be envisaged in organic electronics, since charge carriers can equally by injected from a conjugated semiconductor

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Table 1. Requirements for Thin-Film Nonvolatile Memory Arrays

parameter	value
retention	several (10) years at maximum operation temperature
write time	μs to ms
read time	μs to ms
memory size	strongly application dependent: initial RFID item-level: 8 to 128 bit expectations for smart packaging, cards, toys, badges, e-tickets, wireless sensor nodes, typically 1−64 kbit
write voltage	<24 V
read/write/erase endurance	application dependent: 1×10^3 to $>1 \times 10^6$ write/erase cycles
temperature range	storage: −40 °C to +85 °C operational: −20 °C to +50 °C
density	not critical up to 64 kbit; ~mm^2 or even more per array
integration with logic	desirable for most applications
cost	critical per array, but not necessarily per bit
extra features	integrated on flexible substrates transparent for some applications

into, for instance, a charge-storing gate dielectric (also called "electret"). Charge trapping characteristics can be further optimized by incorporating specific trapping sites in a dielectric, e.g., metal nanoparticles or dispersed charge-accepting (and typically π-conjugated) molecules. Such transistor-based memory concepts have a structure very similar to a normal transistor, which is advantageous for embedding memory in logic, hence satisfying one of the expected requirements of a successful organic nonvolatile memory technology.

In silicon, research to alternatives for flash is fueled by the consensus that the scalability of flash toward nanosized transistors is running into physical limits. Contenders for future technology generations are two-terminal "crossbar" devices in which a material with switchable resistance is sandwiched between two conductive electrodes, forming a vertical switchable resistor (Figure 1). From Table 1, the concern of scalability to nanosized devices is not of prime concern for organic memories. However, the simplicity of crossbar arrays is highly attractive for achieving low cost, and therefore research to switchable resistor crossbar arrays for organic and printed electronics is also a lively field of research. Ultimate scaling of these devices could conceivably even lead to the use of a single molecular layer featuring conductive switching.

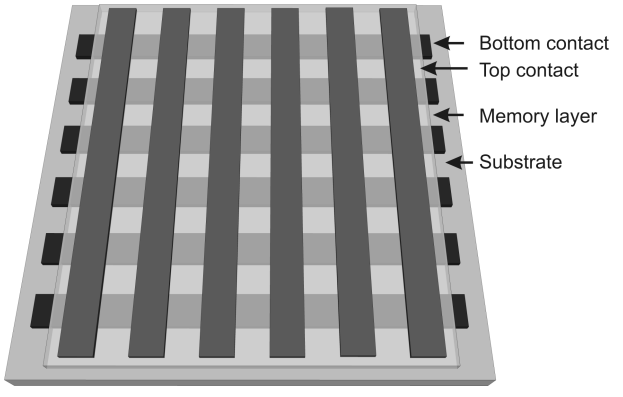

Figure 1. Sketch of a cross-bar memory array with the memory material sandwiched between the bottom contacts (horizontal lines) and the top contacts (vertical lines).

Ferroelectric memories have been extensively investigated as an alternative nonvolatile memory to be integrated with Si.[4] They are based on ferroelectric materials that have two stable states of polarization, leading naturally to a nonvolatile binary (Boolean) system. Ferroelectric perovskite oxides, such as lead zirconate titanate (PZT) and strontium bismuth tantalate (BST) were applied as dielectric of a ferroelectric capacitor in a one-transistor-one-capacitor (1T1C) memory cell, a commercial product today. An alternative ferroelectric memory structure uses a ferroelectric material in the gate stack of a so-called ferroelectric field effect transistor (FeFET). Such device in principle has a better scaling potential than a capacitor, but was found not to be manufacturable in a Si line due to the need of high-temperature oxides and noble electrode materials. Furthermore, silicon transistors require a (thin) SiO_2 dielectric layer between the perovskite oxide and the silicon channel, but the presence of this SiO_2 layer causes depolarization fields and leakage current induced charge compensation that jeopardize the retention time of the Si FeFET. In contrast, polymer ferroelectric memories may prove a viable technology, also in FeFET configuration. Indeed, organic semiconductors are relatively agnostic as to the gate dielectric, and can operate directly on a ferroelectric polymer as gate dielectric without need for an intermediate dielectric, thus reducing the risk of depolarisation. Furthermore, the dielectric constant of ferroelectric polymers is low compared to the giant dielectric constant (100−1000) of typical pervoskite oxides, again reducing the depolarization field in an organic FeFET gate stack compared to that of an oxide FeFET gate stack. Thus, polymer and printable ferroelectric dielectrics are contenders for nonvolatile transistor and capacitor memories. Their prime asset in the list of Table 1 is the long retention of the ferroelectric polarization.

The state of the art of organic memory with the three above concepts is discussed in the paragraphs below. We also outline the challenges that remain to be tackled before these technologies can lead to applications.

2. Resistive Switching Memories

Resistive switching memories come typically in the form of a crossbar cell, in which at least one material with switchable resistance is sandwiched between two electrodes (Figure 1). As mentioned in the introduction, they are main contenders for scaled memory in silicon technologies. However, they have also been actively pursued for thin-film and organic nonvolatile memory device.

2.1. Classification of Resistive Switching Principles and Methods. Figure 2 shows a classification of the physical and chemical principles that can be used to achieve resistive switching.[5] Of these, electronic effects as well as electrochemical effects have been shown with thin-film organic memories.

The method of programming of a resistive memory element is to switch the state of the device from a low conducting OFF state to a highly conducting ON state and vice versa by application of a voltage or current across the electrodes. We can thus make a distinction between unipolar and bipolar switching.

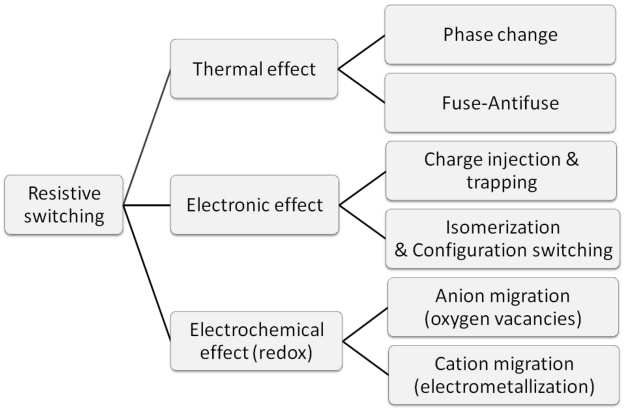

Figure 2. Classification of resistive electrical switching effects for non-volatile memory applications.

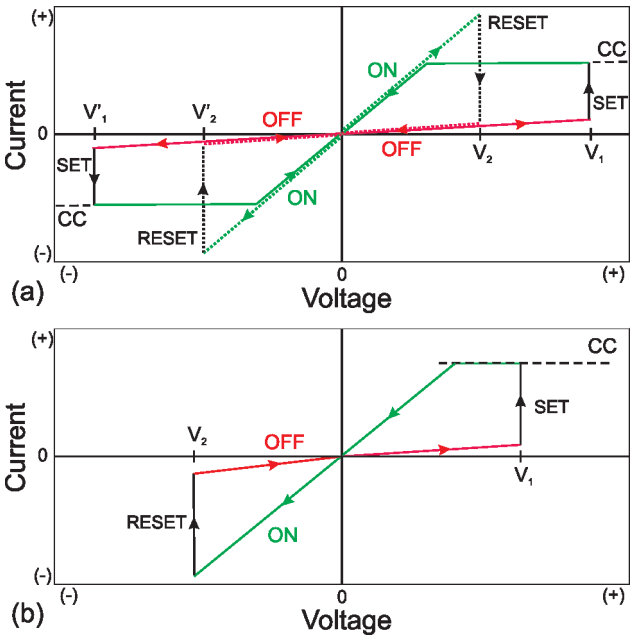

Figure 3. Basic $I-V$ schemes of resistively switching memory cells (linear current and voltage scales). (a) Unipolar switching with the SET operation shown with full line and the RESET operation in dashed line (switching is shown for both polarities). (b) Example of bipolar switching in the case of a memory cell where the SET operation is performed at positive voltages and the RESET operation at negative voltages. CC denotes limitation of the current compliance by a current compliance.

A unipolar device (Figure 3a) is one in which two thresholds with a single polarity of voltage can be defined for the switching. During the SET operation, performed at a voltage V_1 and by limiting the maximum current with a current compliance (CC), the conductivity is switched from LOW to HIGH. The RESET operation (transition from HIGH to LOW conductivity state) is performed at a voltage V_2 where the current across the memory cell (no more limited by the current compliance) is higher than during the SET process. SET and RESET operations are mostly performed at the same polarity (for example respectively at voltages V_1 and V_2, or V_1' and V_2') although it might also be possible to apply a signal of one polarity for the SET, and the other polarity for the RESET process (e.g., V_1 and V_2', or V_1' and V_2). Whereas signals of different polarity might be optionally used for unipolar memories (Figure 3a), their usage is required for bipolar (= reverse polarity switching) memories (Figure 3b). This class of memories requires a signal of one polarity for the SET operation, and the opposite polarity for the RESET operation. To avoid overprogramming (transition to a permanent HIGH conductivity state), the current during the SET operation can be limited by a current compliance or a load resistor placed in series with the memory cell.

The mechanisms giving rise to unipolar and bipolar switching are different, and are discussed in the subsequent paragraphs.

2.2. Molecular Mechanisms. The change in conductivity in these devices can be intrinsic to the employed material, as for example bulk switching or conductivity change of the material, but also extrinsic, as for example when the metal of an electrode takes part in the switching process. Since a large number of polymer and small molecule based organic memories have already been described in recent review papers,[6−8] we will focus here on a discussion of material-related issues affecting the switching process.

Theoretical calculations have shown that intrinsic transformations at the molecular level are in principle capable of generating two stable conductivity states.[9] Referring to Figure 2, we discern different possible molecular mechanisms, including redox (= oxidation−reduction) reactions and isomerization reactions (such as hybridization changes, configuration changes − which include functional group rotation and backbone ring rotation − and others). Isomerization using light (photoisomerization) has been demonstrated for photochromic molecules, and has been shown to allow switching between a high and a low conductivity state, depending upon the wavelength of the irradiation in materials such as diarylethene.[10] It can, however, not be ascertained that this mechanism is operative for devices that are switched electrically. Redox reactions have been proposed as explanation for switching of the storage of electrical charge in self-assembled monolayers with redox-active groups in molecular capacitor memory cells.[11]

2.3. Role of Electrodes and Interfaces. It has proven extremely difficult to ascertain that the switching in many real devices[6−8] is related to these molecular principles rather than to other causes. In some cases, factors such as dust particles[12] or chemical reactions between the memory material and the electrode have been shown to be involved. In many other cases, the switching can be ascribed to an electrode or the electrode/molecule interface. This is especially true in the case of very thin layers of memory materials. For example, molecule-independent switching has been described for Langmuir−Blodgett molecular monolayers made of three very different molecular species (cadmium eicosanoate salt, amphiphilic rotaxane, and the dumbbell-only component of the rotaxane) sandwiched between platinum bottom and titanium top contacts.[13] Another example are Rose Bengal based memory cells, for which initially a mechanism was proposed that involves an electrochemical reaction affecting the molecule conjugation,[14] but where later experiments evidenced the presence of switchable hot spots (highly conductive filaments),[15] as well as switching of memory cells in which the Bengal Rose layer was left out.[16] Similar observations were made with pyrolized

Table 2. Examples of Resistive Switching Inorganic Memories Based on Anion and Cation Migration

type of switching	anion migration (oxygen vacancies)	cation migration (electrometallization)
bipolar	Pt\$TiO_{2-x}$\$TiO_2$\Pt [19] Pt\$TiO_2$\TiN [20] Pt\$MnO_2$\Ti [21] Pt\$ZrO_2$\TiN [22]	Pt\$TiO_2$\Ag [23] Pt\$Ta_2O_5$\Cu [25]
unipolar	Pt\$TiO_2$\TiN [20] Pt\$MnO_2$\Ti [21] Pt\$ZrO_2$\TiN [22]	

photoresist\nitroazobenzene\TiO_2\Ag memory cells, where it was shown that the molecular layer was not required for switching.[17] These results plea against an intrinsic switching mechanism of the organic memory material to explain the observed conductivity switching, but do not rule out that conductivity switching by molecular mechanisms can occur!

In the previous examples, the electrodes proved to play a key role in the switching. In particular, it was observed that crossbar devices of many organic materials (including polymers, semiconductors and insulators) exhibiting conductivity switching comprise an electrode such as aluminum, barium\aluminum, or lithium fluoride\aluminum, which is prone to oxidation.[18] The current in the ON state was shown to flow through conductive filaments. The study permits to conclude that the switching is inherent to the presence of a thin layer of—most often native—aluminum oxide rather than to the organic material (π-conjugated or not). The chemical structure of the polymer influences the read/write voltages but not the yield of operational memories.[18] This links these types of memories to the oxide RRAM memories.[5]

2.4. Conductive Switching in Thin Interfacial Oxide Layers. Since interfacial oxides are essential to explain the conductivity switching of many organic cross-bar memory devices, it is important to classify the types of switching that can occur in such oxide materials. Switching to a high conductivity state has been demonstrated in many metal-oxides, and related to the formation of conductive filaments. Depending on the oxide, two types of filaments can be formed, schematically represented in Table 2.

In oxides such as ZrO_2, MnO_2, and TiO_2, filaments of oxygen vacancies are formed by an electrochemical reaction.[19−22] The formation being by reversible redox reactions, the application of a reverse bias dissolves the filament, at least in part, and hence such memories display bipolar resistive electrical switching. Often, they can also be operated in unipolar programming mode,[20−22] in which case the filament disruption is due to Joule heating. Frequently, the first operation cycle is a "forming" cycle, requiring a higher voltage or longer time, in order to create the first conductive filaments through the otherwise insulating oxide.

In the presence of electrodes with forming monovalent cations (such as Ag^+ and Cu^+), or in oxides and sulfides of such metals (such as CuO, Ag_2S, Cu_2S, ...), filaments of that metal can be formed by electrochemical reduction of the cations at the negatively polarized electrode.[23−26] These devices can be operated in bipolar mode, because the rupture of the conductive metal filaments can be achieved by the reverse electrochemical process at reverse

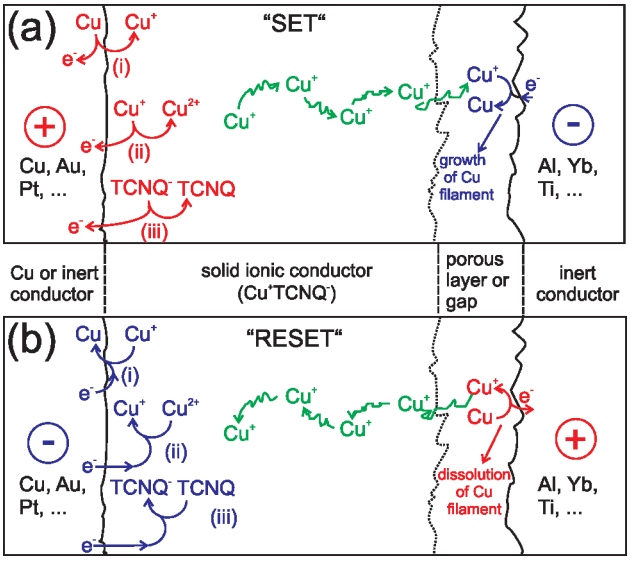

Figure 4. Switching mechanism of CuTCNQ-based organic memories: (a) "SET" operation consisting in formation of a conductive Cu channel by electrochemical reduction of copper ions at the cathode and simultaneous electrochemical oxidation of another species (i), (ii), or (iii) at the anode. (b) "RESET" operation under opposite polarization leading to the dissolution of the conductive channel. Redrawn with permission from ref 28. Copyright 2007 American Institute of Physics.

bias. It is interesting to note that the resistive switching of a Pt\TiO_2\Ag memory cell was attributed to a Ag filamentary conduction path;[23] this might indicate that Ag^+ ion migration might prevail over oxygen vacancy migration.

Parasitic metallic filament formation might also be considered as possible source of resistive electrical switching in memory elements with indium-tin-oxide (ITO) contacts. Indeed, short-circuiting of polymer electroluminescent devices has been related to indium migration from ITO bottom contacts (acting as anode) with consecutive reduction to metallic pathways at the cathode.[27] Because ITO is frequently used as bottom contact in organic memories,[6−8] it may play a role in the observed switching.

2.5. Role of π-Conjugated Materials in the Switching Process. Despite the fact that in most organic cross-bar memories a metal-oxide at the interface is the switching layer and that the switching is caused by conductive filaments (vacancies or metal) in the interfacial oxide, there are nevertheless some cases where the π-conjugated material is believed to play a role in the switching process.

In the case of CuTCNQ (where TCNQ stands for 7,7,8,8-tetracyano-p-quinodimethane) the metal−organic material was proposed to play the role of solid ionic conductor providing mobile Cu^+ cations which form conductive (metallic) filaments by an electrochemical reduction (Figure 4). The reduction occurs at the negative electrode, and the filaments grow in a (porous) oxide layer at that electrode, for example native aluminum oxide.[28] This proposed role of CuTCNQ also explains reported switching of this material when probed with a scanning tunneling microscope tip: indeed, metallic filaments growing from the tip can bridge the nanometer gap between the material and the tip,[28,29] similar to what has been reported for Ag_2S "quantum point contact switch".[26] The similarity between CuTCNQ and inorganic solid ionic conductors

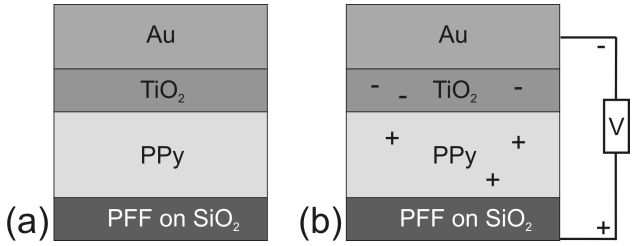

Figure 5. Pyrolyzed photoresist (PPF) on SiO_2\polypyrrole\TiO_2\Au memory cell in (a) OFF state and (b) ON state. Redrawn with permission from ref 37. Copyright 2008 American Chemical Society.

as for example Ag_2S is logic since the organic material fulfills the requirements of good (cat)ionic conductors:[30] (i) it possesses strongly polarizing monovalent cations (as for example Ag^+ and Cu^+), (ii) highly polarizable anions (since the charge in the relatively large π-conjugated system $TCNQ^{\bullet -}$ is highly delocalized), and (iii) 4-, 3-, and perhaps 2-coordination of the cations by the anions (in CuTCNQ the Cu^+ cations are tetracoordinated by the nitrile groups of the $TCNQ^-$ anions[31]). According to this set of requirements, it would be expected that the ionic conductivity of Cu^+ salts with π-conjugated organic anions without nitrile groups should be poorer, and hence memory properties of compounds such as copper tetrachloro-*p*-benzoquinone should be worse than CuTCNQ. Indeed, that expectation has been verified recently,[32] and provides corroboration for the active role of CuTCNQ in the formation of Cu filaments in metal/CuTCNQ/interfacial oxide/metal memories. In addition, the relevance of the porous (oxide) layer was proven by experiments where improved reliability and write/erase endurance was observed for memories made by growing the CuTCNQ onto a dedicated, well-controlled oxide layer.[33,34]

Reproducible electrical switching involving metallic filament formation has also been reported for memory cells where π-conjugated polymers with strongly coordinating heteroatoms such as N and S (as for example poly(3-hexylthiophene), P3HT) were sandwiched between Al bottom contacts and Cu top contacts.[35] In this case, mobile copper ions formed by electrochemical oxidation of the Cu top contact can migrate within the complexing polymer.[35] Because it is quasi impossible to avoid the formation of a thin native AlO_x layer in the case of Al bottom contacts, it might be expected that the switching takes place by reversible Cu filament formation within the thin AlO_x layer, similar to the switching mechanism proposed for CuTCNQ.[28] Alternatively, Cu filament formation can occur in the P3HT layer, as reported for Cu\P3HT\Au diodes,[36] which do not have an oxide layer. It is furthermore noteworthy that the migration of Cu ions in or through a semiconductor as P3HT is reported to be strongly enhanced by elevated relative humidity.[36]

Another principle for nonvolatile organic memories in which an organic semiconductor plays an active role is based on a solid redox electrochemical cell employing polypyrrole and TiO_2[37] (Figure 5). The polypyrrole in contact with the positively biased electrode gets doped (and hence conductive) by electrochemical oxidation, whereas the TiO_2 is reduced to produce electrons into the conduction band. In this case the conductance change in the polymer layer plays a

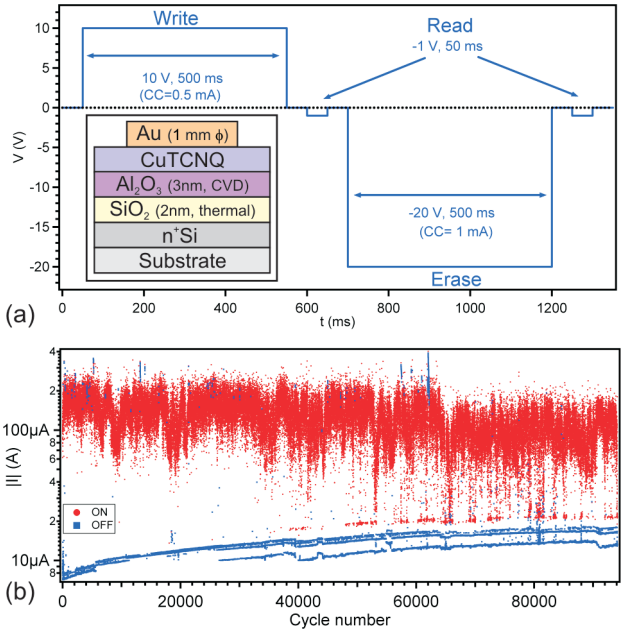

Figure 6. (a) Programming sequence of an inverted CuTCNQ based memory cell[34] with Al_2O_3 and SiO_2 switching layer (CC = current compliance), and (b) reading currents (at −1 V) of the ON and OFF states over more than 90 000 write/erase cycles.

direct role in the conductance change of the memory. Applying a reverse bias pulse returns the resulting conductive junction to its low-conductivity state.

A further principle for resistive switching memories is based on the modulation of the injection barrier at a semiconductor-electrode contact by the means of the polarization field of a ferroelectric material.[38] This promising principle will be detailed further in a dedicated part of this short review.

2.6. Memory Properties of Organic Cross-Bars. One key figure of merit for nonvolatile memories is the endurance to a sufficient number of write/erase cycles (Table 1). Experiments realized on large-area memory cells demonstrated endurance in the range of 1×10^3 to 1×10^5 cycles for CuTCNQ[39,40] (Figure 6) and P3HT[35] based memories. Although these figures are already in the range of those required for some low-cost applications, further research has to be performed toward other requirements such as sufficiently fast switching speed, long retention time, and good temperature stability.

Integration is another key figure for high-density mass storage applications. Although first integrated organic memory cells have been prepared with PEDOT:PSS (WORM memory)[3] and CuTCNQ[41,42] as well as an analogous copper-based charge-transfer complex,[43] additional research is required in order to improve electrical properties (endurance, switching speed, retention time, etc.) as well as on the material side in order to avoid thermal degradation of the organic material during the encapsulation process.

Finally, it should be noted that read-out of the memory state in a resistive cross-bar memory is known to be limited by so-called sneak current paths,[44] which cause a false reading of the reading of the conductivity state of a junction because of leakage currents in the surrounding

crossbar network. To reduce sneak currents, it is known that a selecting device, such as a diode, has to be placed in series with the conductive switching device. Therefore, it can be highly beneficial that the conductive switching device would inherently possess rectifying characteristics, as for example possible with diodes containing a blend of an organic semiconductor and a ferro-electric polymer,[45] which will be discussed in section 4. It should also be mentioned that addressing unipolar switching devices is simpler than addressing bipolar memory devices, because for the latter, the switching of the memory devices requires polarity reversal of the addressing circuitry.

2.7. Summary and Outlook. Several mechanisms may cause the electrical conductivity of molecules to switch. However, in real devices comprising a thin film of such molecules, the switching is mostly due to the formation of conductive filaments in an interfacial oxide.

Therefore, only in a few cases could a role in the switching be ascribed to the organic semiconductor. This is the case in solid-state redox cells as well as in semiconductor ferroelectric diodes.

3. Charge-Storage in Transistor Gate Dielectric

Organic nonvolatile memory devices based on organic field-effect transistors (OFETs) are especially attractive, because these devices can be read without destruction of their memory state ("non-destructive read-out") and have a manufacturing advantage because of their architectural compatibility with integrated circuits composed of OFETs. Moreover, integration of transistor devices solves the sneak current problem, which most frequently occurs in a passive crossbar array of memory elements.[46]

Transistors have three electrodes, the source, the drain, and the gate. Organic transistors utilize π-conjugated organic molecules as semiconductor channel between source and drain. The semiconductor channel is separated from the gate by a thin gate dielectric layer. Charge carriers can be accumulated at or repelled from the interface between semiconductor and gate dielectric by the gate bias (V_g). When accumulated, the charge carriers form a conductive channel between source and drain, and current (I_d) can flow upon application of a drain bias. The gate thus controls the OFET as a switch, and the threshold voltage (V_{Th}) is defined as the voltage to be applied at the gate to start forming a conductive channel. Beyond the threshold voltage, the surface density of carriers is proportional to the difference between V_g and V_{Th}. Transistors can be integrated into logic gates and circuits.[47] The type of π-conjugated organic molecules utilized in the channel of the OFETs and the sign of the gate potential determine whether the primary type of charge carriers are electrons (giving rise to so-called "n-type transistors") or holes ("p-type transistors").

3.1. Operation of Charge-Storage OFET Memory Devices. Accumulated charges in the transistor channel are fundamentally "volatile", i.e., only present as long as an attracting gate voltage in excess of V_{Th} is applied. Such a transistor can have memory properties if either reversible charge trapping or detrapping can be made to occur in the gate dielectric layer.

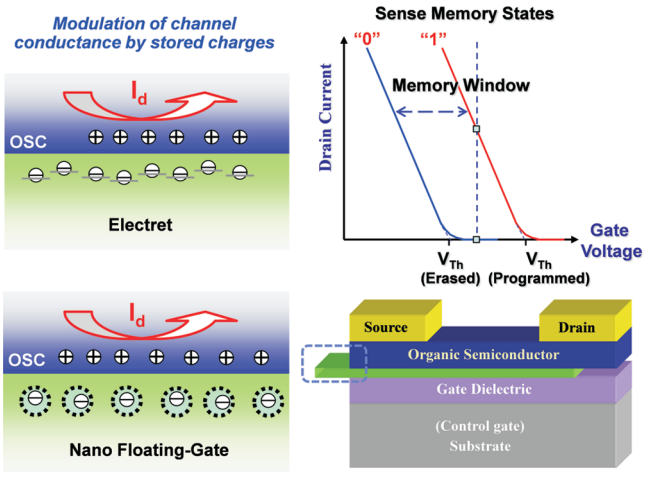

Figure 7. Schematic configuration and operational mechanism of an organic memory p-type transistor device.

Several types of gate dielectrics enable reversible trapping of charges upon application of a gate field, for instance polymer electrets, dielectrics with embedded metallic or semiconducting nanoparticles (NPs) or organic conjugated molecules, and ferroelectric gate insulators with permanent and/or switchable electrical dipoles.[8] In this section, we introduce the basic properties, operational mechanisms, and recent progress in memory devices based on OFETs with gate insulators that have charge-storage capacity.

Charge trapping in the gate dielectric causes the threshold voltage (V_{Th}) of the transistor to shift.[48] The magnitude of the shift in V_{Th} is proportional to the stored charge density per unit area Δn:

$$\Delta V_{Th} = \frac{e\Delta n}{C_i} \quad (1)$$

where e is the elementary charge and C_i is the capacitance of the gate dielectric per unit area. This shift is visualized by plotting the transfer curve of the transistor – this is the drain current (I_d) as a function of gate voltage (V_g) at constant drain voltage (V_d) – for the fresh device and for the transistor with charged gate dielectric. The gate voltage shift between these curves is the memory window. As shown in Figure 7, there are two different current states for each V_g within the memory window, namely a high I_d and a low I_d, representing the "1" and "0" of the memory, respectively. Here, one should distinguish the memory behavior from bias-stress effects in OFETs by defect states or impurities in semiconductor and/or gate dielectrics, which also leads to V_{Th} shifts.[49] Although this external effects would enhance to be opened memory window, it cannot be controllable to use as a practical memory as well as not permanent. The memory is nonvolatile if the V_{Th} shift is (quasi) permanent as long as the state of the device is not intentionally overwritten. The memory transistor is rewritable if the programmed state can be reversibly recovered to its original state by application of an appropriate (re)programming bias. Programming is preferably done by shifting V_{Th} such that two distinct memory states are created at zero V_g, ideally the two states correspond to a positive and a negative V_{Th}. Indeed, that allows to read out the memory

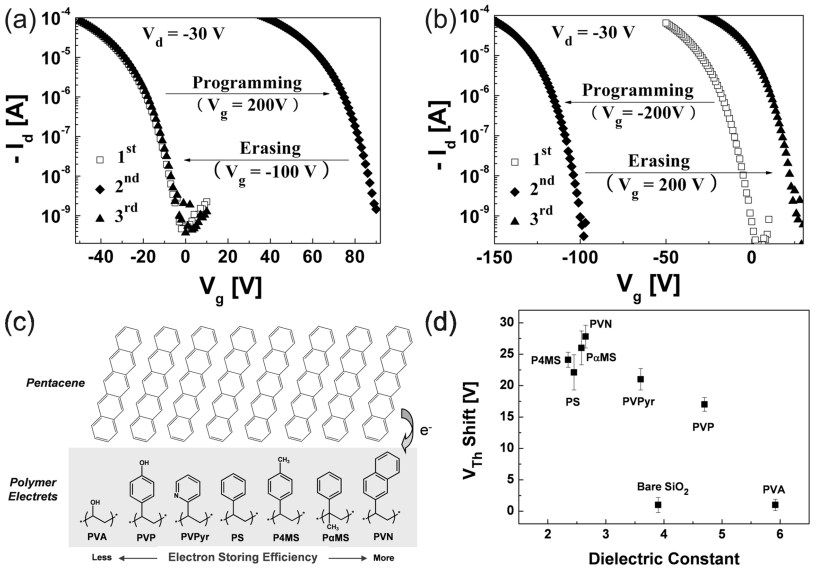

Figure 8. Shifts in transfer plots at $V_d = -30$ V in the (a) positive and (b) negative directions for a pentacene OFET memory device with a 300 nm thick SiO_2 layer.[53] (c) Schematic representation of the electron-storage efficiency of electret materials (d) Relationship between V_{Th} shifts and the dielectric constant.[54] Reproduced with permission from refs 53 and 54. Copyright 2006 and 2008 Wiley-VCH Verlag GmbH & Co. KGaA.

states at zero V_g without need to apply a potentially destructive gate field. In addition, it enables low power consumption and reliable data storage. The charge-storage mechanisms in the gate dielectric layer OFET-based memory devices can be classified into three types: (i) charge-trap memory, (ii) floating-gate memory, and (iii) ferroelectric memory. The ferroelectric memory transistors will be described in the next section of this article, thus only floating-gate and charge-trap-based OFET memory are discussed in this section.

3.2. Charge Storage in Polymer Electret. An electret is defined as a dielectric material that has a quasi-permanent electric charge or dipolar polarization, including ferro-, piezo-, and pyro-electric polymers.[50,51] Polymer electrets have been utilized in a wide variety of applications such as transducers, electrophotography, optical display systems, gas filters, and motors because of their ability to store charges for a relatively long time.[50,51] Katz et al. first demonstrated a memory transistor based on an OFET configuration with a polarizable gate insulator.[52] Both p-type 1,4-bis(5-phenyl-2-thienyl)benzene (PTPTP) and n-type *N*,*N*′-bis(1H,1H-perfluorooctyl) naphthalene-1,4,5,8-tetracarboxylic diimide (F_{15}−NTCDI) OFETs were shown. Switching of V_{Th} from the accumulation mode to either zero or the depletion mode was demonstrated by application of a depletion voltage (i.e., positive V_g for p-type semiconductors and negative V_g for n-type semiconductors) to the gate electrode. The PTPTP and F_{15}−NTCDI semiconductors were chosen because they are typically normally on OFETs, i.e., the initial V_{Th} is positive for the p-channel PTPTP and negative for the n-channel F_{15}−NTCDI OFET. As chargeable gate dielectric, two inorganic materials [SiO_2 and glass resin] and two hydrophobic polymers [poly(4-methylstyrene) (P4MS) and cyclic olefin copolymer] were used. The hydrophobic polymer dielectrics showed better memory characteristics because of their superior charge-storage (electret) properties. However, the memory device required a relatively long switching time (∼10 min).

Baeg et al. reported an advanced memory transistor with pentacene and a dual gate dielectric, composed of poly(α-methylstyrene) (PαMS) and SiO_2.[53] This memory device showed a very large memory window with a relatively long retention time greater than 100 h (Figure 8a,b). The long retention time indicates that mobile charge carriers transferred from pentacene were deeply trapped in the PαMS layer or at the interface between PαMS and SiO_2. The device exhibited a very short switching time (up to ∼μs). In experiments using various styrene-based polymer electrets, the same group also showed the importance of using polymer electrets to obtain stable memory behavior (Figure 8c).[54] Systematically controllable and reversible shifts in the transfer plots were only observed in OFETs with nonpolar and hydrophobic polymer electrets, such as polystyrene (PS), PαMS, P4MS, and poly(2-vinyl naphthalene) (PVN). Moreover, the magnitude of the memory windows was inversely proportional to both the hydrophilicity and polarity of the dielectrics [Figure 8d]. Recently, Debucquoy et al. observed that holes trapped in the gate dielectric of p-type OFETs are more easily erased by overwriting trapped holes by electrons injected from the semiconductor channel (at positive V_g) than by detrapping of holes.[55] This signifies that reversible switching of the memory requires the (nominally p-type) semiconductor to be to some extent ambipolar, i.e., some amount of mobility is required for both types of charge carriers, electrons and holes, in the semiconductor. As hydrophilic and polar polymer dielectrics are known to create electron traps at the semiconductor−dielectric interface that hampers ambipolarity,[56] this observation is an explanation why dielectrics such as poly(vinyl alcohol) (PVA) and poly(vinyl phenol) (PVP), form poorer memories. Furthermore, it was also noticed that strong ambipolar transport in the semiconductor can result in bidirectional V_{Th} shifts, and therefore large memory windows and smaller programming fields.[55]

The programming voltage is dictated by the minimum gate field required to induce charge carrier tunneling into

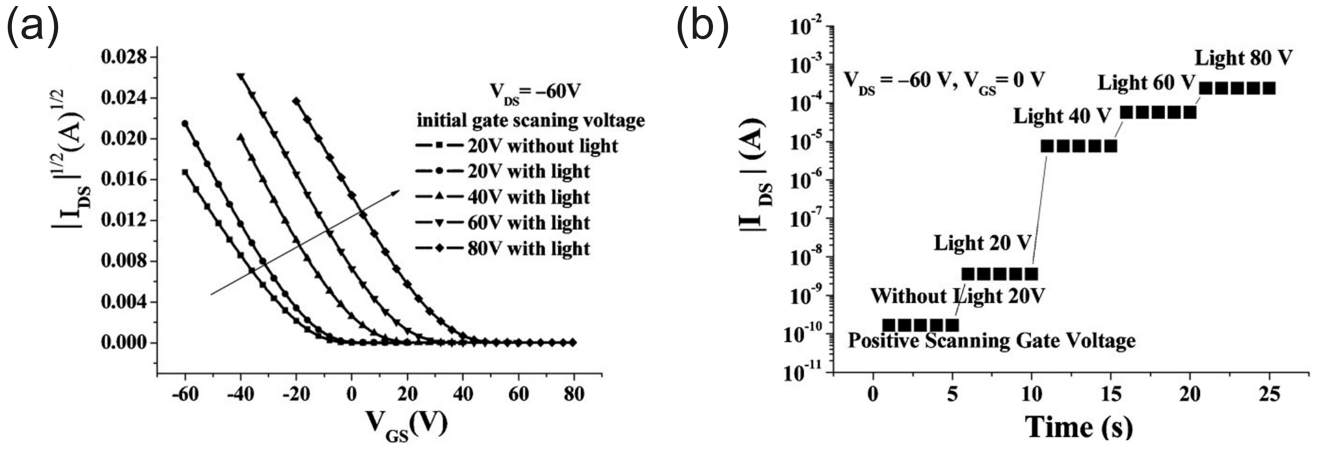

Figure 9. Transfer characteristics of devices that use a light-assisted programming. (a) $|I_{DS}|^{1/2}$ versus V_{GS} and (b) the corresponding different current levels at $V_{GS} = 0$ V and $V_{DS} = -60$ V for a pentacene FET modified with a PS layer. Reproduced with permission from ref 58. Copyright 2009 Wiley-VCH Verlag GmbH & Co. KGaA.

the polymer electret. Initial work reported relatively high programming voltages, as a result of the use of a thick SiO_2 layer. Recently, a device with a low operating voltage was demonstrated using very thin dual gate dielectrics—a 20 nm thick SiO_2 layer and a 4 nm thick PαMS layer. This memory device could be written and erased at voltages as low as 15 V.[57]

The programmability of OFET-based memory devices with organic electrets is not limited to single-level storage. Guo et al. reported multibit pentacene or copper phthalocyanine (CuPc) transistor memory with PS (or PMMA) on SiO_2 through light-assistant programming.[58] Application of different magnitudes of gate bias in combination with bias light was used to control the magnitude in the shifts in V_{Th} and V_{on} (Figure 9). A unique feature of this memory device is that many charge carriers were supplied by the bias light, whereby the resulting excitons were separated by application of the appropriate V_g. The mobile electrons and holes were captured in a thin polymer electret layer that was configured as a high-energy-electron tunneling layer (or a hot-electron injection layer) and a barrier layer to inhibit low-energy electron tunneling.[58] Multibits memory is very attractive because of the significant increase in memory capacity per unit cell area. Other interesting memory transistors using trilayered cross-linked PVP (cPVP), PVA or biopolymers, such as deoxyribonucleic acid (DNA), as a chargeable dielectric layer have been demonstrated.[59−62]

3.3. Nanoparticle-Embedded Gate Dielectrics. Another type of charge-trapping OFET memory is organic floating-gate memory.[63] In this device, charges are stored in a metal or in a semiconducting layer called a floating gate, located within the insulating gate dielectric, and completely surrounded by insulator (Figure 7). Charges are injected on the floating gate from the transistor channel by application of high V_g. They cause a V_{Th} shift, similarly as in the case of charge trapping in the insulator. To discharge the floating gate, a reverse bias is applied at the gate electrode. The magnitude of the V_{Th} shift depends on the density of the trapped charges in the floating gate.[64] Floating gate memories can be fabricated using a variety of insulating polymers as the controlling and tunneling gate dielectric.

Silicon flash memories often use a floating gate electrode, but this geometry has not been demonstrated so far for organic memory transistors.[8] An alternative, also pioneered in silicon, is to embed conducting nanoparticles (NPs) in an insulating gate dielectric matrix.[65,66] Each particle is a charge-storage site independent and isolated from other sites. This is more robust against loss of charge as compared to a floating gate.

Au NPs have a high chemical stability and can be formed and processed from solution.[66] Zhen et al. reported an all-organic NP floating gate memory device with CuPc as an active channel and e-beam-deposited Au NPs inside a polyimide gate dielectric layer.[67] Holes were injected from CuPc into the Au NPs by application of a negative gate bias by Fowler-Nordheim tunneling. The stored charges could be expelled from the Au NPs into the CuPc under the positive gate bias to erase the memory. Mabrook et al. demonstrated a device that gets away with e-beam to form the Au NP's, and instead uses solution-processed Au NPs formed by a self-assembled dipping method on poly(methyl methacrylate) (PMMA).[68] However, in this device the Au NPs were positioned directly in contact with the (pentacene) transistor channel, leading to spontaneous leakage of the stored charge and hence a poor retention. Kim et al. incorporated Au NPs under a tunneling dielectric layer (PMMA or PVP/HfO_2), so that the transistor active layer (pentacene) is isolated from the Au NP floating gate.[69] The Au NP's were deposited by means of layer-by-layer (LbL) deposition on positively charged poly(allylamine hydrochloride) (PAH), as part of a PAH/PSS(poly(styrenesulfonate)) multilayer dielectric. On top of this stack, a tunneling layer of HfO_2 separated the Au NPs from the pentacene channel. This device exhibited significant shifts in V_{Th} and a large memory window of 3 to 5 V after application of V_g of 50−70 V with a relatively long retention time (several months). A similar approach was used for solution-processable, conjugated polymers. Liu et al. reported a P3HT, floating gate memory transistor using electrostatic LbL self-assembly of Au NPs.[70] However, the retention time was as short as ∼200 s, presumably because of the poor insulating properties of the PVP barrier layer.[54] Baeg et al. reported a solution-processed

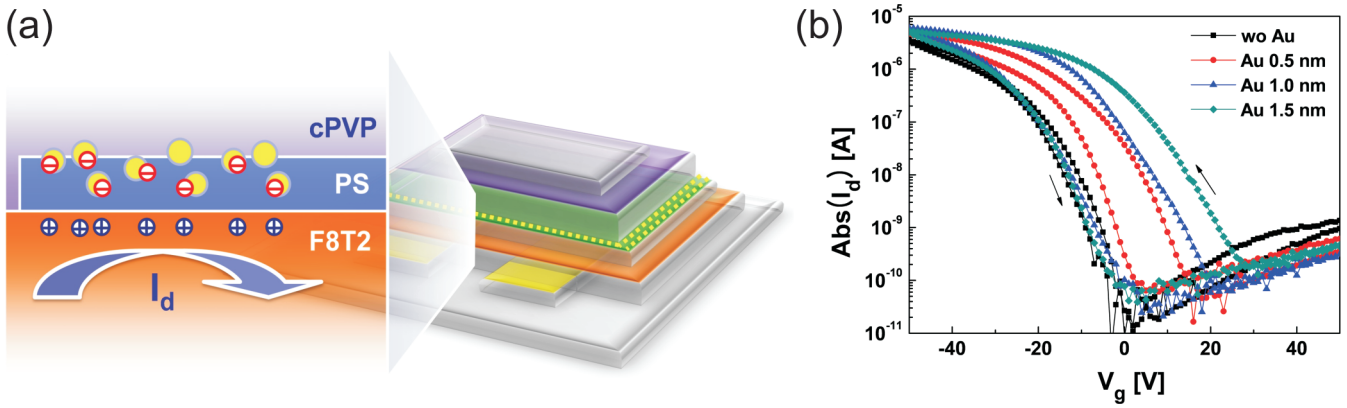

Figure 10. (a) Schematic device configuration of a top-gate/bottom-contact F8T2 floating gate memory transistor and the charge-trapping mechanism in Au NPs. (b) Transfer characteristics of F8T2 OFET devices after thermal evaporation of Au of different thicknesses, ranging from 0.5 to 1.5 nm, where V_g was varied from 90 V to −90 V. Reproduced with permission from ref 63. Copyright 2010 Wiley-VCH Verlag GmbH & Co. KGaA.

poly[9,9-dioctylfluorenyl-2,7-diyl]-co-(bithiophene)] (F8T2) transistor with a top-gate/bottom-contact configuration [Figure 10] with Au NPs incorporated between bilayered dielectrics PS and cPVP.[63] A flexible polymer memory device was also fabricated on a PET plastic substrate, operating as well as those on glass.

To decrease the operating voltage of these devices, the thickness of the gate dielectric film must be reduced, while the density of NPs must be increased to increase the memory window. However, these conditions are not easy to fulfill without producing electrical shorts or a severe leakage current through the gate dielectric layer. One promising idea is to embed high-density Au NPs into the dielectric film at low-temperature using an in situ micellar block-copolymer as a template for the metallic NPs. The metal NPs synthesized in situ in one block of a diblock-copolymer template enabled the production of homogeneous and high-density NP arrays only within a certain area of the film. Leong et al. reported an OFET memory using Au NPs self-organized in polystyrene-block-poly-4-vinyl-pyridine (PS-b-P4VP) block copolymer nanodomains.[71] Both p- (pentacene) and n-channel (perfluorinated copper phthalocyanine, F_{16}CuPC) OFETs showed stable programmable and erasable properties due to charge confinement in the embedded Au NPs.

π-Conjugated molecules have also been incorporated into gate dielectrics as charge-storage sites, similar to metal NPs floating gate devices. Common π-conjugated molecules have electron-donating or -accepting properties so that an OFET threshold voltage can be controlled by charge trapping on the π-conjugated molecules embedded in the dielectric layer. Wu et al. achieved memory transistors by use of a donor-polymer-blend as a buffer layer between a CuPc active semiconductor channel layer and a SiO_2 gate dielectric.[72] Various organic donor molecules, such as tetrathiafulvalene, ferrocene, or 5,10,15,20-tetraphenyl-21H,23H-porphine nickel(II), were blended with conventional insulating polymers, including PMMA, poly(ethylene oxide) or PS. Charging and discharging in the donor-polymer blend layer were demonstrated. The charging effect was reported to be due to an electric-field-induced charge transfer between CuPc and the organic donors. The retention was longer than 24 h. The operation voltage and the memory window were adjustable by changing the thickness of the dielectric layer, and could be scaled to 2 V. Baeg et al. demonstrated a similar device using a PVP and PCBM blended film, in which PCBM molecules were incorporated as an electron traps. The V_{Th} of pentacene OFETs showed reversible and systematic shifts after application of external gate fields[73] resulting from electron trapping and detrapping on the PCBM molecules. Recently, it was proposed to graft C_{60} as charge-capturing molecule onto self-assembling phosphonic acid molecules,[74] thus making electrically programmable self-assembled molecular gate dielectric layer wich can be assembled on aluminum oxide. The gate dielectric consisting of oxidized Al and memory SAM was estimated to be only 5.7 nm, resulting in low programming voltages of 2 to 3 V. The C_{60} units were separated from the transistor channel by the alkyl side chains (0.9 nm) of α,α'-dihexylsexithiophene molecules used as semiconductor. That small separation was responsible for a short retention time (6 h).

3.4. Summary and Outlook. Various strategies were shown to achieve trapping and detrapping of charges in a gate dielectric of an OFET. Despite the many demonstrations, several issues remain to be solved before these principles can be utilized in flexible low-end commercial applications: (i) the reliability of the memory operation, (ii) lowering of the high operating voltage, and (iii) increasing the retention time. The density of charge-storage sites has to be thoroughly understood and optimized. The operating voltage is related to the capacitance (and thickness) of the dielectric layers. Currently, there are clear limitations to the use of very thin blocking and tunneling layers as a result of the penetration of metal ions and/or generation of pinholes. For safe data storage and long retention time, research on robust mono- or bilayered dielectrics is required, as they are generally preferable to hydrophobic and nonpolar materials for ultralow leakage characteristics.

4. Polymer Ferroelectric Devices

Ferroelectrics are polar substances of either solid (crystalline or polymeric) or liquid crystal, in which spontaneously generated electric polarization can be reversed by inverting the external electric field. Mathematically, ferroelectric

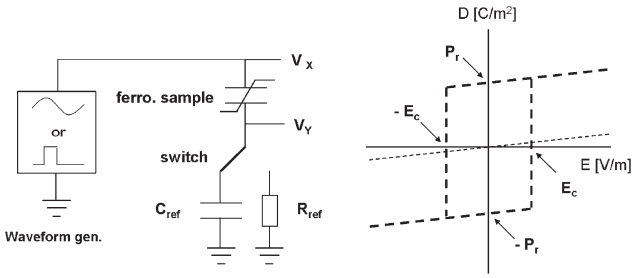

Figure 11. Right: Hysteretic loop of ferroelectric thin film between two electrodes. The displacement (D) of the dielectric is given by the sum of free charges ($\varepsilon_r E$) and polarization (P), with E the externally applied electric field. The slope of the line is the dielectric constant of the material and characterizes the charging of the capacitor. In this idealized case, the remanent polarization, P_r, can adopt two opposing values (positive and negative), the absolute magnitudes of which are equal and constant. They are interchanged instantly at a distinct externally applied field, the coercive field E_c. For $-E_c < \mathbf{E} < E_c$, the capacitor may contain different charges (polarizations) at each E. Left: Measurement of $D-E$ hysteresis and transient switching phenomena using a Sawyer−Tower setup.[75]

polarization can be described by the equation

$$D = \varepsilon_r E + P$$

with P the polarization, D the dielectric displacement and E the electric field. ε_r is the relative permittivity of the dielectric material. The spontaneous polarization P originates from the alignment of intrinsic dipole moments inside the material. The direction of these dipoles can be changed up or down depending on the direction of the applied external electric field. The critical electric field for reversing the polarization in a ferroelectric is called a coercive field. The electric displacement as a function of field strength consequently draws a hysteretic curve ($D-E$ loop) between opposite polarities, and this electric bistability can be used, for example, for nonvolatile memory elements. In particular, ferroelectric random access memory (FeRAM) and ferroelectric field-effect transistors are current targets for practical applications$_3$.

A standard method for measuring the $D-E$ loop is with a Sawyer−Tower circuit (Figure 11).[75] A sinusoidal voltage signal is applied to one of the electrodes of the ferroelectric capacitor and the amount of charge displacement in the other electrode is measured using the voltage it creates over a reference capacitor connected in series. A idealized $D-E$ hysteresis curve is shown in Figure 11 for a ferroelectric capacitor with two parallel electrodes. At a low voltage, only a linear component is measured: the field is not large enough to affect P. At higher fields, a hysteretic response develops which saturates at even higher fields. P_r is the remanent polarization defined as the polarization after removing the external electric field ($E = 0$) and E_c is the coercive field, which is the field needed to reduce the polarization to zero ($P = 0$). P_r and E_c are the main parameters describing the ferroelectric characteristics of the material. A ferroelectric with a high coercive field yields a higher memory window ($2 E_c d$, where d is the thickness of the ferroelectric), but this is at the expense of higher voltages that are necessary for switching. A ferroelectric with a high remanent polarization P_r leads to higher switching currents in capacitors and currents in transistors,[76] but cannot be fully polarized using low voltage operation, so subloops are used that are less stable.

4.1. Materials. In 1969, Kawai first observed the piezoelectric effect in a polymer, polyvinylidene fluoride (PVDF).[77] Two years later, the ferroelectric properties of the same polymer were reported. Throughout the 1970s and 1980s, these polymers were applied to data storage and retrieval. After the discovery of PVDF, many other polymers have been sought after that contain ferroelectric properties. Initially, different blends and copolymers of PVDF were investigated, such as a PVDF with poly(methyl methacrylate).[78] Other polymers were discovered to possess ferroelectricity, such as polytrifluoroethylene,[79] copolymers of VDF and TrFE, and odd-numbered nylon.[76,80−82]

Small molecule organic ferroelectrics are rare,[83] possibly because polarization reversal requires reorientation of the whole molecule within tight crystalline structures. A notable exception is formed by liquid crystalline materials. They switch at low electric fields and are therefore used in displays. For memory purposes their low P_r values is unfavorable.

Table 3 lists the ferroelectric parameters of the most studied organic ferroelectric materials. Also included are the parameters of the two inorganic ferroelectric materials that are currently studied most: $SrBi_2Ta_2O_9$ (SBT) and $PbZrTi_{1-x}O_3$ (PZT). Both are used in memories. They are of perovkite structure and have a high dielectric permittivity (high-k) of ~250 in thin films.[84] Hybrid organic−inorganic composite materials are also explored and have characteristics dependent on the loading of the inorganic nanoparticle.

From this table, it is clear that PVDF and the copolymers of VDF and TrFE have several advantageous properties including a relatively large remanent polarization and a short switching time. By contrast, ferroelectric nylons, for example, have a switching time that is longer by orders of magnitude at the same applied field.[78] Hence, the properties of PVDF and P(VDF-TrFE) will be further discussed.

The ferroelectricity of PVDF and P(VDF-TrFE) stems from the dipole moments in the molecule that can be aligned with the applied field by a rotation of the polymer chain, as illustrated in Figure 12. The dipole moments originate predominantly from the presence of the strongly electronegative fluorine atoms. The dipole switching involves rotation of the dipoles around the backbone. It depends strongly on temperature and the strength of applied field.[80] This already implies that preferred chain configuration is all-trans. This phase is referred to as the β-phase. Due to an optimal alignment of all the C−F dipole moments in the crystal unit cell, this phase gives the highest ferroelectric response.

When PVDF is processed into a thin film, either from the melt or from solution, it adopts the so-called α-phase: the polymer chains have alternatively trans and gauche conformation,[78] which cancels out the overall polarization. To confer ferroelectric properties to PVDF, it is usually mechanically stretched and/or electrically poled to orient the molecular chains in the all-trans conformation (β-phase). Other methods to realize this phase involve addition of hygroscopic salts, epitaxy on KBr, control of cooling and

Table 3. Parameters of Ferroelectric Materials

material class	material	E_c (MV/m)	P_r (mc/m^2)	switching time (s)
inorganic perovskites	$SrBi_2Ta_2O_9$ $PbZrTi_{1-x}O_3$	< 5	100−500	$< 1 \times 10^{-8}$
polymer	vinylidene difluoride based polymer	50−60	50−90	1×10^{-5}
	odd-nylons	70	50−90	100
	poly(thio)urea	40	300	100
molecule	liquid crystals	0.2	5	?
composite	polymer loaded with inorganic particles	intermediate	intermediate	intermediate

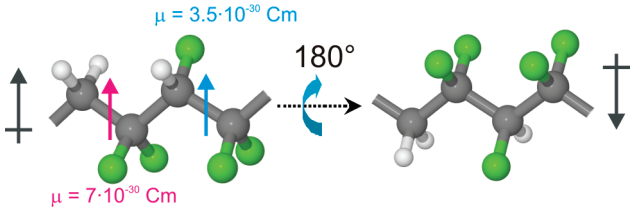

Figure 12. Chemical structure of P(VDF-TrFE) and ferroelectric switching mechanism. In the ferrroelectric phase the dipole moments of the C−F bonds in the VDF monomer and TrFE monomer are aligned as a result of the all-trans conformation of the carbon−carbon backbone of the polymer. The net dipole moment of the VDF monomer is 7×10^{-30} Cm and of the TrFE monomer is 3.5×10^{-30} Cm. When a sufficiently large electric field is applied the polymer chain rotates 180° around its axis, effectively aligning the dipole moments in the other direction. This switching mechanism can be used to store information in the memory device. Carbon, hydrogen, and fluorine atoms are respectively colored in black, white, and green.

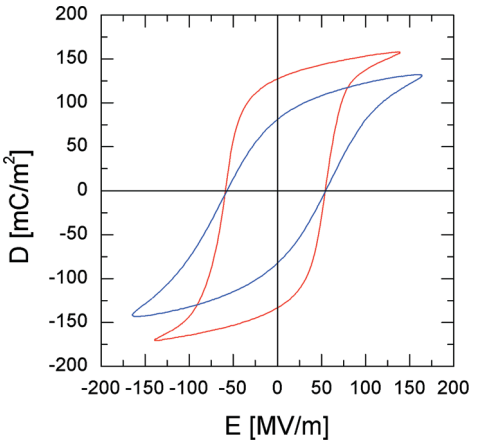

Figure 13. $D-E$ hysteretic loop of P(VDF-TrFE) films with different VDF to TrFE ratio. In blue, the molar ratio VDF:TrFE was 50:50. In red, it was 80:20.

heating rate, solvent evaporation rate, as well as blending with poly(methylmethacrylate).[85−90]

The copolymerization of PVDF and PTrFE is an efficient way to obtain the β-phase. The one larger fluoride atom in PTrFE monomer that replaces the smaller hydrogen atom in the PVDF monomer induces a strong steric hindrance, which spontaneously induces the all-trans conformation. Generally the β-phase can be obtained for molar ratios 50−80% of VDF by introducing TrFE monomers directly. No additional processing is needed.[91]

The crystalline polymorphs of P(VDF-TrFE) are dependent on the temperature. The ferroelectric compounds demonstrate ferroelectricity only below a certain phase transition temperature, called the Curie temperature, T_c, and are paraelectric above this temperature. T_c ranges from 70 to 140 °C. The Curie temperature is lower than the melting point T_m. which decreases from 160 to 140 °C in the VDF range of 60 to 80%. To improve the crystallinity and thereby the ferroelectric response, solution cast P(VDF-TrFE) is thermally annealed in the paraelectric phase (above Curie temperature) for some time. Thermal motion promotes molecular chains to rearrange their positions and form a highly crystalline state.[92]

Figure 13 shows $D-E$ hysteresis loops of random copolymers of VDF and TrFE with different TrFE content. Indeed the one with less TrFE displays a higher P_r. Note that E_c is not affected by a differing TrFE content.

The steric difficulty in reorienting dipoles in PVDF and P(VDF-TrFE) gives rise to a large coercive field (50−60 MV/m) compared with other ferroelectrics. Thin layers are therefore required in order to achieve low-voltage memories. Research on thin film ferroelectrics has made substantial progress. In 1998 Bune et al. have made P(VDF-TrFE) films as thin as 1 nm by Langmuir−Blodgett deposition, that can be switched with as little as 1 V.[79] These results suggested that P(VDF-TrFE) is a suitable candidate material for low-voltage memory applications. The coercive field and polarization switching time was however strongly increasing with decreasing thickness.[81] A number of studies confirmed these results, and the deterioration of ferroelectric properties was attributed to a reduction of crystallinity, as determined by X-ray diffraction experiments.[93−95] However, several groups independently reported low-voltage switching in thin P(VDF-TrFE) layers with a remanent polarization, coercive field and switching time behavior similar to that of bulk P(VDF-TrFE). These reports clearly pointed out the role of the electrode used. In commonly used aluminum electrodes an interfacial defect layer between the ferroelectric and the metal is formed, independent whether the aluminum is above or below the ferroelectric layer. This "dead" layer is nonferroelectric and its relative influence becomes stronger as the ferroelectric film thickness is reduced. By using other electrode materials such as chemically more inert Au,[96,97] Ni[98] or the conductive polymers poly(3,4-ethylenedioxythiophene)[99] or polypyrrole[100] doped with poly(styrene sulfonic acid), the P(VDF-TrFE) layer thickness can be reduced to 50−65 nm to attain low voltage switching, without any obvious degradation of ferroelectric response. Particularly noteworthy is the work of Fujisaki et al.[101] They prepared 60 nm-thick P(VDF-TrFE) capacitors with P_r of 11.9 μC/cm^2 and V_c of 2 V.

Kim et al. fabricated capacitors with different sub-100-nm P(VDF-TrFE) thicknesses to operate below 10 V and measured the switching and retention properties.[97] It was demonstrated that a voltage pulse longer than 80 μs is needed to maintain data, which means that P(VDF-TrFE) capacitors can be operated at 6.25 kHz (inverse of 160 μs).

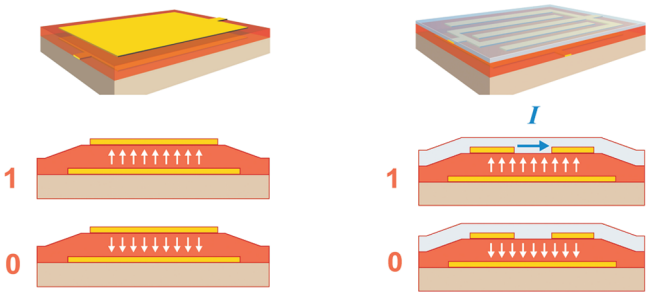

Figure 14. FRAM (left) and FeFET (right) basic cells.

The maximum operating frequency can be increased by applying a larger electric field, albeit at the expense of electrical breakdown probability. Films with a layer thickness of 40 nm or less suffered from poor retention times. It was stated that "memory devices operating at low voltages are hard to be realized because of the roughness of the semicrystalline polymer; therefore, a breakthrough to reduce the surface roughness of P(VDF-TrFE) is required". In their devices, the surface roughness depended on film thickness and the rms roughness was 1.97 nm for a 40 nm thick film, 2.69 nm for a 60 nm thick film, and 3.03 nm for 90 nm thick sample.

By blending PVDF and PMMA followed by melt quenching from 200 °C, films with very low surface roughness were made and electrically characterized in capacitors as well as transistors.[102] PVDF was chosen over P(VDF-TrFE) because of its higher Curie temperature. Films were studied with a thickness of around 200 nm. Addition of PMMA resulted in smoother films. The surface roughness was found to decrease from 5.1 nm for pure PVDF film with a-crystals to approximately 1.7 nm with 10 wt.-% PMMA, and approximately 0.45 nm with 60 wt % PMMA. Unfortunately, the remanent polarization charge was negatively affected. It decreased with the increase of the PMMA fraction, from 4.8 mC/cm^2 for a blend ratio of 90:10 to 0.25 mC/cm^2 for a ratio of 40:60. Optimal composition was therefore chosen to be 80:20. Retention time and switching characteristics were not reported.

Very recently, it was shown that by nanoembossing P(VDF-TrFE) film, the orientation of the crystallographic axes and the crystal quality of the ferroelectric layer can be easily controlled.[103] This resulted in ideal square-shaped and narrow hysteresis loops, with a coercive field of 10MV/m, i.e.. well below bulk values, thereby providing compatibility with low-voltage technologies.

4.2. Principles of Memory Operation. In ferroelectric-based memories, information is stored via the polarization state. Polarization in one of two directions is interpreted as "0" or "1". In FRAM, the ferroelectric is used as a capacitor in the configuration shown in Figure 14. The FeFET is derived from the 1T-1C (one transistor−one capacitor) FRAM basic cell by integrating the ferroelectric in the gate stack of the select transistor below the gate electrode, thus resulting in a smaller basic cell. Because of the smaller cell, a higher integration density is possible. Moreover, as will be shown further on, this new structure enables a nondestructive read out.

4.2.1. Capacitor. In its simplest form, a ferroelectric capacitor is a ferroelectric layer sandwiched between two electrodes. By applying a sufficiently large bias, the ferroelectric layer is polarized in one of two possible states. The polarization state can be read (or better: inferred) by detecting the amount of charge build up during a certain time period (t) by measuring the voltage over a reference capacitor with respect to ground using an integrating circuit. Depending on whether the polarization was aligned or not with the direction of the applied field, a low or a high charge displacement current response is measured. If the directions of the internal polarization and the applied field were opposite, readout changed the polarization state and the stored information is altered. Therefore, it is necessary to rewrite the memory cell to its original state after read-out. In other words, the read-out protocol for capacitor based memories is destructive. It requires relatively complex read-out circuitry, that becomes increasingly difficult when the capacitor's size is downscaled. Furthermore, because readout is destructive, the memories should withstand a high number of write-rewrite cycles (endurance).

An interesting result in this respect is the frequency dependence of a metal/P(VDF-TrFE)/metal capacitor in which the driving voltages with lower frequency and higher amplitude correspond to higher endurance, or less fatigue. Zhu et al. have proposed a universal scaling behavior with N/f, where N is the number of switching cycles and f is the frequency in the fatigue behavior originating from the trapped charges, injected from electrodes into polymer films (Figure 15).[104]

Compensation charges in the metal stabilize the polarization at the surfaces of the ferroelectrics. If charge compensation is complete, the electric fields in and outside the material are zero and the polarization state is pertained even when no bias is applied anymore. Hence, the information is stored for an infinite amount of time. If, however, compensating charge cannot move into close proximity to the ferroelectric surface, for instance, because of an interfacial defect layer, compensation is not complete. Effectively, a nonzero depolarization field is formed that negatively affects the remanent polarization charge and data retention time. Even a few percent of uncompensated polarization charge results in a significant suppression of measured ferroelectric properties.[105] This depolarization effect becomes stronger as the ferroelectric film thickness is reduced. This explains why it is difficult to realize low-voltage memory capacitors with good data retention, and points to the importance of electrode interfaces, as was described above.

Reduction of the capacitor area is desired to increase the memory density. However, the average current during switching scales with P_r, capacitor area A and switching time t as $I = (P_rA)/t$; therefore, a reduction in area reduces the signal response. This imposes requirements on the read-out circuitry.

4.2.2. Field-Effect Transistor. The simplest layout of a FeFET comprises a metal-ferroelectric-semiconductor layer stack (Figure 14), in which the ferroelectric layer serves as the gate dielectric. Sometimes another dielectric layer is inserted between the semiconductor and the ferroelectric.

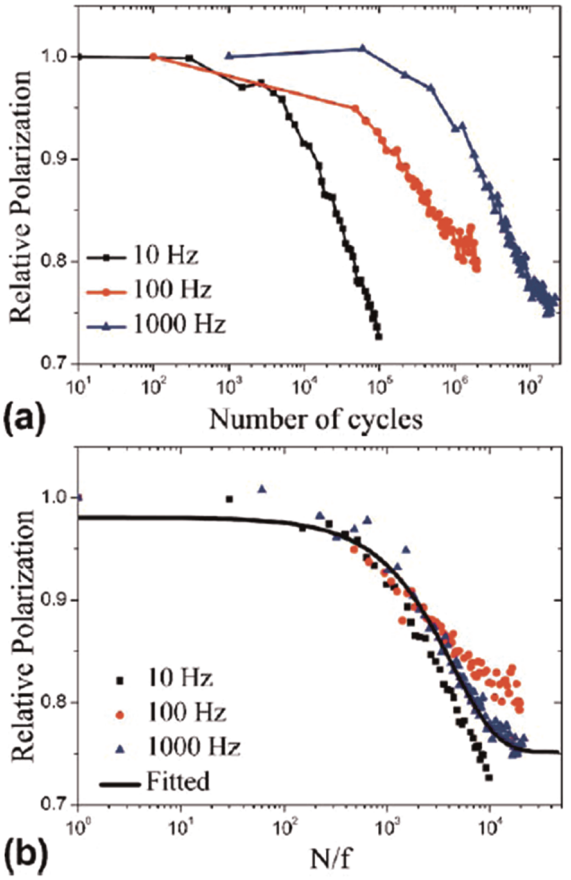

Figure 15. Normalized remanent polarization of 1-mm thick P(VDF-TrFE) sandwiched between Al and Au electrodes as a function of logarithm of (a) the number of cycles (N) and (b) N/f, where f is the frequency of fatigue voltage. Reprinted with permission from ref 104. Copyright 2006 American Institute of Physics.

The ferroelectric layer, because of its remanent polarization, can adopt either of two stable polarization states. These states persist when no biases are applied, i.e., at power shutdown. Switching from one polarization state to the other can occur by applying a sufficiently large gate bias. Depending on the direction of the polarization, positive or negative counter charges are induced in the semiconductor at the semiconductor-ferroelectric interface, effectively causing a positive or negative onset voltage shift of the transistor. Hence, a gate bias window, defined by the shifted onset voltages, exists wherein the drain current may have either of two levels depending on the actual polarization state of the ferroelectric gate dielectric. The corresponding drain current levels can be used to define Boolean "0" and "1" states of a nonvolatile memory with nondestructive read-out.[76] This is illustrated schematically in Figure 14. Nondestructive read-out provides the advantage that the memory is not subjected to the destructive read/rewrite cycle commonly employed in ferroelectric capacitor memories, so the lifetime of the device is limited only by the number of times the memory is written.

In 1986 the first FeFET based on a polymeric ferroelectric was demonstrated. It was shown that ferroelectric polarization within a film of a random copolymer of vinylidenedifluoride and trifluoroethylene, P(VDF/TrFE),[78] could induce an inversion layer in a bulk silicon semiconductor substrate.[106] Thin-film FeFETs using an inorganic ferroelectric and a p-type organic semiconductor were reported by Velu et al. and Kodzasa et al.[107,108] The inorganic ferroelectric layer in these devices requires processing temperatures above 600 °C. This makes the process incompatible with the use of plastic substrates. The ratio of remanent channel conductance of the on and the off state was approximately 10. No switching times or data retention times were reported.

In 2004, all-organic FeFET devices incorporating a ferroelectric-like polymer as the gate insulator and pentacene as the organic semiconductor were first reported by Schroeder et al.[109] The ferroelectric-like polymer is a nylon, poly(*m*-xylylene adipamide) "MXD6".[78] A clear hysteresis in transfer characteristic was observed with an ON/OFF ratio of 200 at $V_g = -2.5$ V, and 30 at $V_g = 0$ V. Retention time was around 3 h. Unni et al. fabricated a pentacene FeFET memory with P(VDF−TrFE) (70:30) as the gate insulator.[110] He reported similar values for the ON/OFF ratio and retention time. In a follow-up paper, the MXD6 deposition was improved leading to much better memory characteristics.[111] ON/OFF increased to 10,000. Data retention increased from hours to days. Switching speeds were not reported. The programming time can however be estimated to exceed 200 ms, typical for nylons.[78] On the basis of the switching time alone, one would clearly favor P(VDF-TrFE) over MXD6 as ferroelectric of choice. On the other hand, MXD6 is amorphous which may be potentially beneficial lead to a smoother interface with the semiconductor, which is particularly relevant for charge transport and low-voltage operation (implying thin ferroelectric).

In both cases, pentacene was used as active semiconductor. Pentacene was deposited using vacuum processing. High-performance solution-processed polymer FeFETs were first reported in 2005 by Naber et al. using P(VDF−TrFE) (65:35) as the gate insulator and MEH-PPV (poly [2-methoxy-5-(2-ethyl-hexyloxy)-*p*-phenylene-vinylene]) as a semiconductor.[112] Identical FETs were prepared with nonferroelectric PTrFE as the gate insulator. These devices did not show appreciable hysteresis, whereas those made with P(VDF−TrFE) show hysteretic drain currents with an ON/OFF ratio at zero gate voltage of 10^4 or higher, leading to the conclusion that the ON/OFF ratio and hysteresis are the result of channel current modulation as a result of poling of the ferroelectric. By directly comparing the transfer curves of the P(VDF-TrFE) and PTrFE transistors, it was estimated that the ferroelectric poling induced a remanent surface charge density of 18mC/m^2 in the semiconductor channel. The polymer FeFETs have a retention time >1 week, a programming cycle endurance >1000 cycles) and a short programming time (OFF to ON, 0.3 ms; ON to OFF, 0.5 ms).[112]

With 60 V and higher, the operating voltages of Naber's FeFETs were relatively high. To reduce the programming voltage and the gate insulator, thickness should be scaled down. However, when using thin films, a great deal of attention needs to be paid to the interfaces, electrodes and sample quality for devices to work reliably. In capacitors, using PEDOT:PSS as electrode material results in superior characteristics, particularly at low P(VDF-TrFE) layer

thickness. Therefore, Gelinck et al.[113] fabricated all-polymer FeFETs using thin P(VDF-TrFE) films sandwiched between electrodes (gate and source/drain) made of conducting PEDOT:PSS. The electrodes were patterned by photoexposure of the deposited films. Alkoxy-substituted polyphenylene vinylene derivative, OC1C10, was used as p-type semiconductor and PCBM, a C_{60} derivate, was used as n-type semiconductor. All layers were solution processed by spincoating. The technology was scaled up to a wafer size of 150 mm. For both unipolar p- or n-type semiconductor channels, the transistors have remanent current modulations of $\sim 1 \times 10^3$ with a retention time of hours. They can be switched in 0.1−1 ms at operating voltages less than 10 V. By measuring the switching current as a function of channel length, the remanent polarization charge was estimated to be 6 mC/m^2.

Since then, several groups reported organic FeFET based on pentacene and P(VDF−TrFE) as the gate dielectric. Different approaches have been proposed that in one way or another improve the ferroelectric/semiconductor interface (reduced surface roughness leads to higher mobility) and/or leakage current. Nguyen et al. stretched P(VDF-TrFE) thin films to simultaneously enhance the crystallinity and lower the surface roughness.[114] The FeFET had a mobility of 0.1 cm^2/(V s). The drain current on/off ratio was 1×10^4. Recently, a method was described to fabricate ferroelectric β-type PVDF thin films on Au substrate by the humidity controlled spin-casting combined with rapid thermal treatment. A FeFET with the β-PVDF shows a drain current bistability of 100 at zero gate voltage with ±20 V gate voltage sweep and a higher thermal stability than P(VDF-TrFE), up to 160 °C.[88] A cross-linkable interlayer inserted between gate electrode and PVDF-TrFE layer significantly reduced the gate leakage current, leading to source−drain OFF current of approximately 1×10^{-11} A. The corresponding FeFET device shows a clockwise $I-V$ hysteresis with drain current bistability of 10^3 at ±40 V gate voltage.[115] A bottom gate FeFET containing PVDF/PMMA (80/20) blend films of 200 nm thickness with low surface roughness exhibits an on/off bistability ratio of 1×10^4 with data retention capability over 15 h at an operation voltage of 15 V.[102] In that work, polycrystalline and single crystalline 6,13-bis(triisopropyl-silylethynyl) pentacene (TIPS-PEN) was used as the active semiconductor. Because the low surface roughness was equal or lower than the width of the accumulation layer, charge transport in the accumulation layer was not inhibited significantly, as evidenced by the high field effect mobility of 0.65 cm^2/(V s).

Naber et al. also addressed the issue of surface roughness.[116] A top gate configuration was used so that the semiconductor-ferroelectric interface roughness is not determined by the top surface of the P(VDF-TrFE) but by that of P3HT. By further optimizing the P3HT thin film processing a surface roughness of only 0.7 nm was obtained. This turned out to be a key factor in order to achieve a polymer FeFET with both high charge mobility (0.1 cm^2/(V s)) and high charge density (28 mC/m^2). MIS diode measurements with P3HT as active layer demonstrate that the bistability in these devices originates from switching between two states in which the ferroelectric gate dielectric is either polarized or depolarized. Pulsed charge displacement measurements of these diodes in the polarized state give accumulated charge values of 40 ± 3 mC/m^2.[117]

Top gate FeFETs having an amorphous conjugated polymer, poly(9,9-dioctylfluorene-co-bithiophene) (F8T2) as active channel material exhibit near perfect yield due to their smooth surface morphology. The transfer curves of the fabricated TFTs exhibited counter-clockwise hysteretic behaviors, which is a result of the ferroelectric poling. Memory transistors using Ni/P(VDF-TrFE)/F8T2 exhibit promising behaviors such as a memory window of 2.5 V at V_G of 5 to −10 V, four orders of magnitude of ON/OFF ratio, and gate leakage current of 1×10^{-10} A.[118]

Top gate configuration has also been used successfully by several groups in combination with (transparent) n-type metal oxide semiconductors. Metal oxide-based TFTs have at least 1 order higher mobility (10−50 cm^2/(V s))[119] than amorphous Si-TFTs and organic TFT. The candidate materials attracting the most interest can be broadly divided into two oxide categories. The first group is zinc oxide (ZnO),[120] and the second is amorphous oxides with heavy metal content, such as amorphous InGaZnO (a-IGZO).[121] Both pass visible light and are almost completely transparent. Besides the high mobility, oxide-based TFTs have other advantages such as room temperature deposition, better smoothness, etc. The latter makes them particularly amenable to integration into top gate FeFETs for simple and low cost memory devices using large-area electronics technology. Top gate ZnO FeFET has been reported by several groups.[122−124] Noh et al. employed a poly (4-vinylphenol) (PVP)/P(VDF-TrFE) double layer gate dielectric which shows remarkably reduced leakage current with the aid of the PVP buffer layer. The device exhibits a field effect mobility of 0.36 cm^2/V and a large memory hysteresis in the transfer characteristics with the data retention longer than 2 h.[122] A solution-processed nonvolatile memory transistor was demonstrated using zinc indium oxide (ZIO) as active channel material and P(VDF-TrFE) as gate dielectric.[125] The semiconducting active channel of zinc indium oxide was prepared by spin-coating from a precursor solution. The obtained ZIO film was amorphous and optically transparent. The voltage shift originating from the ferroelectric polarization resulted in a high ON/OFF ratio of 8×10^6 at 20 V gate and drain bias. This high value was the result of both a high ON-current, related to the high field-effect mobility of 1.3 cm^2/(V s), and low leakage currents in the OFF state. The ON-OFF decreased to ~500 after 10 h.

Fully transparent memory transistors were made using oxide semiconducting Al−Zn−Sn-O (AZTO) layers and ITO electrodes.[126] A 6 nm thick Al_2O_3 layer was in between the AZTO and P(VDF-TrFE) layer to protect the AZTO during the coating and etching processes of P(VDF-TrFE). All the fabrication processes were performed below 200 °C. With a gate voltage sweep of −10 to 10 V, the ON/OFF ratio was 1×10^8. The field-effect mobility and gate leakage currents were obtained to be 32.2 cm^2/(V s) and 1×10^{-13} A,

respectively. All these characteristics correspond to the best among all types of nonvolatile thin-film memory transistors reported so far. Switching, retention and endurance characteristics were discussed extensively, showing that programming speed (> 500 ms) and retention time (~1 h) should be improved further.

4.3. Application and Outlook for Ferroelectric Memory Devices. Ferroelectric polymer materials perform well enough for relatively simple memory applications. First products will most likely be relatively large ferroelectric capacitors that can be written and read using external conventional driving electronics using ca. 20 V. Typically, tens of memory bits are produced using low-cost reel-to-reel printing processes on thin plastic foils that can be integrated into game cards, toys, etc.

With increasing size, matrix-addressed memory architecture is advantageous. In these arrays, all of the bits are subjected to at least one-half of the probing voltage. Under such conditions, the ferroelectrics would exhibit a finite probability of switching their polarization state, a problem known as the "half-voltage disturb effect." The relative importance of the disturb effect increases when scaling down the size of the bits, which on the other hand is economically attractive. This disturb problem can be solved by adding a transistor to each memory cell so that the write voltage can reach the ferroelectric memory element and alter its polarization state only when the transistor is activated. This pass-transistor architecture is now common in inorganic FRAM. The second issue is the switching voltage itself. Low-voltage capacitors with good retention properties are difficult to realize. By far the most serious difficulty with capacitor-based ferroelectric memories is fatigue, which is a drop in the polarization with progressive switching. A related issue is imprint, which is a preference of the ferroelectric storage element to remain in (or go back to) one of the two states. Both of these problems are related to the electrode/ferroelectric interface.

Regarding the FeFET, the retention loss problem is the number one issue at the moment. Widespread use of nonvolatile memories in production systems requires data retention for ten years or more, a challenging requirement to meet. Low carrier density in the semiconductor can result in insufficient charge near the ferroelectric/semiconductor interface, leaving a residual depolarization field that negatively affects data retention time. Although both fatigue and imprint are likely to apply in the case of the FeFET too, the remedy will probably lie, as with ferroelectric capacitors, in the improvement of the interfaces. Also, the transistor-type memories are yet to meet the high-density and low-cost requirements. So far, only one case of FeFET integration into arrays has been reported.[123] Sekitani et al.[127] reported a 8×9 matrix of P(VDF-TrFE)-based FeFETs. These achievements are important steps toward cheap and viable nonvolatile memories.

Recently, nonvolatile bistable rectifying diodes were made using phase-separated films of P(VDF-TrFE) and the polymer semiconductor rir-P3HT [regio-irregular poly(3-hexylthiophene)] with a LiF/Al top contact and a silver bottom contact. A memory architecture based on a blend of semiconducting and ferroelectric polymers has been reported.[45] The thin-film blends show a columnar morphology, with P3HT-rich columns enclosed in a continuous, essentially pure P(VDF-TrFE) phase.[128] The concept behind this memory element is to combine two polymers that have distinct roles in the device operation: a ferroelectric polymer provides the binary state and data retention whereas a semiconducting polymer provides the means to probe that state via an electrical signal. The polarization field of the ferroelectric modulates the injection barrier at the semiconductor−electrode contact and, hence, the resistance of the diodes. Switching and data retention times were comparable to best values reported for FeFETs. In a systematic follow-up study the polymer semiconductor as well as electrode materials were varied. It was demonstrated that injection barriers up to 1.6 eV can be surmounted by the ferroelectric polarization yielding on/off current modulations of more than 5 orders of magnitude.[38]

The diode allows for a simple crossbar array. The resistance of the memory switches, and hence the device offers the possibility for simple current read out. To exploit such a memory device in a flexible electronic circuit, a number of fundamental and technological hurdles need to be overcome: understanding and improvement of the device operation needs to be developed, as well as the influence of and process control over the nanoscale morphology of the blends.

4.4. Summary. Devices based on ferroelectric capacitors are close to commercialization.

Ferroelectric OFETs currently have the best performance among thin-film transistor-type memories. Because of their similar architecture, they can be integrated into existing technology based on organic transistors. This compensates, to some extent, for the larger footprint of the device. Key to achieving good performance is the formation of well-defined, abrupt interfaces, especially between semiconductor and gate insulator. A challenge in this respect is that P(VDF-TrFE) polymers are semicrystalline and thin layers therefore are relatively rough. Depolarization, which reduces the retention, is a second concern.[129]

5. Conclusions

This paper reviewed the various types of nonvolatile memories based on π-conjugated compounds. We highlighted the role of the materials in the memory functionality, with the intention to provide helpful indications for further improvement of the material properties.

The role of the π-conjugated semiconductors in (nonvolatile) memory devices was shown to depend on the type of memory used. In resistive switching memories, the mechanism of switching is most often based on filament formation by electrochemical processes. In one class of those devices, a solid-state ionic conductor is needed in which metal cations are transported that form metal filaments growing at the negatively polarized electrode. π-Conjugated organic materials can be very suitable solid-state ionic conductors because delocalization of the negative charge inside the system

Table 4. Comparison of the Types of Polymer Memories Classified by Their Primary Circuit Elements (reworked from ref 8)

type	MIM-type	transistor-type (OFET)	resistor-type (MSM and FE diode)
physical description	Capacitor stores charges of opposite polarity on plate electrodes. Each bit is stored in a separate capacitor.	Charge storage and/or polarization at the dielectric-semiconductor interface modulates channel current of the transistor. Level of channel current indicates the bit level of the OFET memory.	Data storage is based on the high and low conductivity (bistability of resistance) of resistor in response to the applied electric field.
device structure	(a) metal−ferroelectric−metal (MFM) (b) metal−insulator−ferroelectric−metal (MIFM)	(a) floating gate (b) charge trapping dielectric (c) ferroelectric as gate dielectric	(a) MIM = metal−insulator−metal (b) MSM = metal−semiconductor−metal (c) MISM = metal−insulator−semiconductor−metal (d) M\S:FE\M = metal−semiconductor:ferroelectric blend−metal
materials	ferroelectric polymers: PVDF or P(VDF-TrFE), odd nylons, cyano polymers, poly(thio)ureas, FLC polymers	(a) FET semiconductor: π-conjugated polymers/molecules, metal oxides (b) gate dielectric: inorganic insulators, polymer dielectrics, polymer−polymer blends, composites with nanoparticles, insulators with blended donor or acceptor molecules, ferroelectric polymers	interfacial oxides, insulating polymers (also with nanoparticles), semiconducting polymers and small molecules (also with NPs), solid-state ionic conductors, composite materials, ferroelectric:semiconductor blends
mechanism	ferroelectric polymer maintains permanent electric polarization that can be repeatedly switched between two stable states by an external electric field.	charge storage or polarization in OFET gate dielectric gives rise a shift of V_{Th} or hysteresis, creating bistable transistor transfer curves	electrical bistability of resistance by (a) creation and annihiliation of filaments (metallic or oxygen vacancy); (b) redox doping/dedoping of a semiconductor; (c) switching of carrier injection in a semiconductor
memory cell	(a) one (pass) transistor +1 capacitor (1T1C) (b) one (pass) transistor +2 capacitors (1T2C) (c) two transistors +2 capacitors (2T2C)	(a) one memory transistor (1T)'NAND flash, NOR flash, DRAM' (b) one pass transistor +1 memory transistor (2T)	(a) one memory diode (1D) (b) one diode +1 memory resistor (1D1R) (c) one pass transistor +1 memory resistor (1T1R)
performance factors	polymer composition, crystallinity, film thickness, switching dynamics, film defects, metal electrodes, field pulses, fatigue characteristics	charge mobility, capacitance per area, maximum electric displacement, impurity, morphology, crystal packing, energy barrier, deposition conditions	filamentary conduction, filament rupture, electrode materials, control of interfaces and interfacial oxides, redox doping effects, carrier injection at electrodes
status	close to commercialization	research	research
technical limitations	(a) destructive read-out (b) material degradation (fatigue) (c) capacitor scaling	(a) thickness and roughness control of dielectric layer (b) parasitic capacitance (c) depolarization and retention time	(a)mechanisms unascertained (b) retention time and temperature stability of conductive filaments (c) complexity of programming of bipolar memories (d) sneak current paths in resistor arrays

promotes cation mobility. Another switching mechanism based on π-conjugated materials that was found to be very promising is based on electrochemical doping and dedoping of a conjugated semiconductor at an electrode interface. A third category of resistive switching memories employ a blend of an organic semiconductor and a ferroelectric polymer. The conductivity switching is obtained by switching the charge injection barrier between the electrode and the organic semiconductor. As a consequence, the memory properties depend on the charge-transport properties as well as on the location of the electronic levels of the organic semiconductor. A second class of memory devices are transistors with conjugated semiconductors as channel material, in which the memory effect relies on charge trapping in the gate dielectric or ferro-electric polarization of the gate dielectric. In these devices, the obvious role of the π-conujugated material is the transport of the charges needed to switch the memory state, as well as for reading out the memory state. It is noteworthy that for such devices, it can be advantageous to use ambipolar semiconductors, which can provide both types of charge carriers into the channel. Furthermore, some examples were provided where organic semiconductor molecules are used within a charge-trapping layer as charge trapping sites.

We summarize in Table 4 the main characteristics of the devices and architectures discussed in the paper. Each of

memory classes has potential, but also remaining issues to be solved. Commercial applications are expected to be reached with ferroelectric capacitor memory banks first. Transistors are expected to simplify mainly the read-out, as they allow to remove the constraint of destructive read-out. Despite the fact that many parameters of Table 1 have been shown separately for memory transistors, the integration of all parameters in one FET technology is not proven. Also the retention time of these devices still requires attention.

Vertical resistive-type memories are most attractive toward high integration density. The switchable diodes in addition provide a solution to the sneak current problem. These technologies require further work to acquire maturity, as indicated in Table 4.

In addition to the further development of memory devices, the integration with thin-film transistors circuitry for read-out and programming is a subject of further research. This is expected to lead to memory banks integrated in applications not served by present-day silicon nonvolatile memory technology.

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